**Max Score = 15 points**

CS 250 2018 Spring Homework 10

This assignment is due at 11:59:00 pm Thursday, April 12, 2018.

Insert your typewritten answers into this file. You may include images of neatly hand drawn diagrams when appropriate. To have this assignment graded, upload your file to Blackboard in either PDF or Word format. You may upload more than once to permit correction of errors. Late submissions will receive a score of zero (0).

You are responsible for ensuring that your upload (1) is to the location in Blackboard for this assignment, and (2) is the file that you intend to have graded for this assignment, and (3) is not marked “LATE” by Blackboard. You are encouraged to verify your upload was successful by downloading your file from Blackboard and examining that download.

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1. Text exercise 14.4  
   If the interface width is 16, is the interface parallel or serial? Explain

Parallel.

Interface width is 16 means number of parallel wires an interface uses is 16 rather than a serial interface design which only two wires are used for data transmission.

1. Text exercise 14.7  
   If the interface between a processor and storage device has a width of thirty-two bits, how

can the processor transfer a data item that consists of sixty-four bits?

We use multiplexor. Break sixty-four bits into thirty-two bits chunks and send one chunk a time to multiplexing hardware.

1. Text exercise 14.9  
   Suppose a serial interface has a latency of 200 microseconds. How long does it take to transfer one bit over the interface? How long does it take to transfer sixty-four bits over the interface?

200\*1 = 200 microseconds

200\*64=12,800 microseconds

1. Text exercise 15.1  
   A hardware architect asks you to choose between a single, thirty-two bit bus design that multiplexes both data and address information across the bus or two sixteen-bit buses, one used to send address information and one used to send data. Which design do you choose? Why?

I think I will choose a single, thirty-two bits bus design for data and address because firstly multiple buses can be expensive and complicated, secondly data and address are strongly related, syncing between two buses of data and address can be dangerous. Single 64 bits takes 2 transactions, and dual 16-bits takes 4 transactions.

1. What are the two types of bus error?  
   Address conflict

Unassigned address

1. Run a system info command on your computer and use its output to find three different buses that your computer contains. For each bus, (1) describe in specific detail the physical hardware from which it would be constructed, (2) name the units within your computer that are connected to the bus (if any) and the external units (if any) typically connected to the bus, (3) classify the bus as serial or parallel, (4) state if the bus is proprietary or if is it standard and when was its standard specification released and what entity released the spec, and (5) state how the bus addresses are configured (manually per I/O device, by hardwiring on the bus, or automatically), and (6) state for automatically configured buses, state whether the bus is hot-pluggable or not. The web, especially Wikipedia, can be a helpful resource.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Bus name | From where | Connected units | Serial/parallel | Proprietary? /  Standard: When and by whom? | How addresses are configured? | Automatically configured buses? Hot-pluggable? |
| PCI | Those PCI slots on motherboard | Network/Sound/video card | Parallel | Intel  Conventional PCI was created on June 22, 1992 | 0x80000000 | bus << 16 | device << 11 | function << 8 | offset | Yes  No |
| ISA | Those ISA slots on motherboard | Peripheral cards to motherboard | Parallel | IBM  1981 |  | Yes,  Yes |
| USB | Those USB ports on motherboard | Keyboard, mouse, flash drive, USB cable | Serial | Compaq, DEC, IBM, Intel, Microsoft, NEC, and Nortel  January 1996 |  | No,  Yes |

1. Text exercise 15.9  
   10^6\*8/2^20 = 7.62
2. Text exercise 15.11  
   Min(n,m)
3. Text exercise 16.1  
   1/0.002 = 500
4. Text exercise 16.5  
   mouse is slower than disk, so disk has higher priority.
5. Text exercise 17.4

Because information is stored in queue, which is volatile.